

Maybe help page

By Avishai Adler (2001)

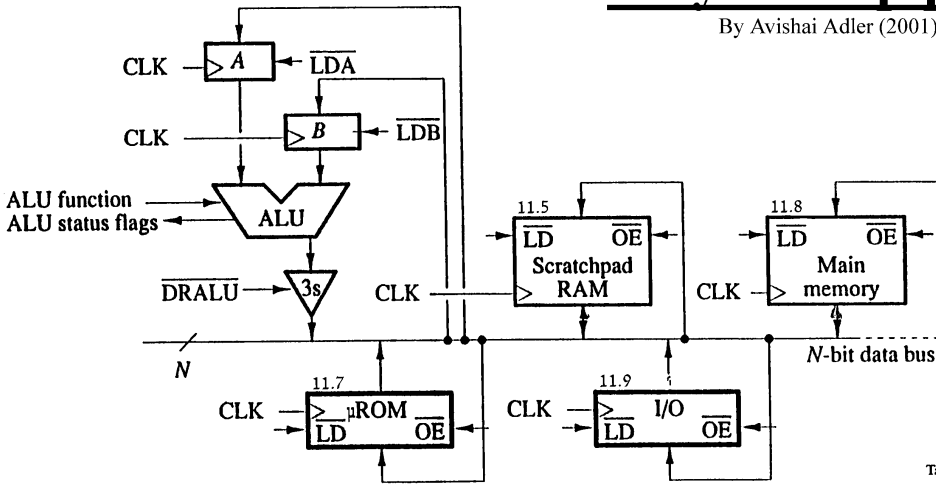


Figure 11.2 Microinterpreter data paths.

Table A2.1 Control-ROM output word.

Address increment	ALU inputs	N.C.	COND S/L	Drive select	Load select
ADR+	F ₃ F ₂ F ₁ F ₀ C̄ M	X	I S	D ₂ D ₁ D ₀	L ₂ L ₁ L ₀

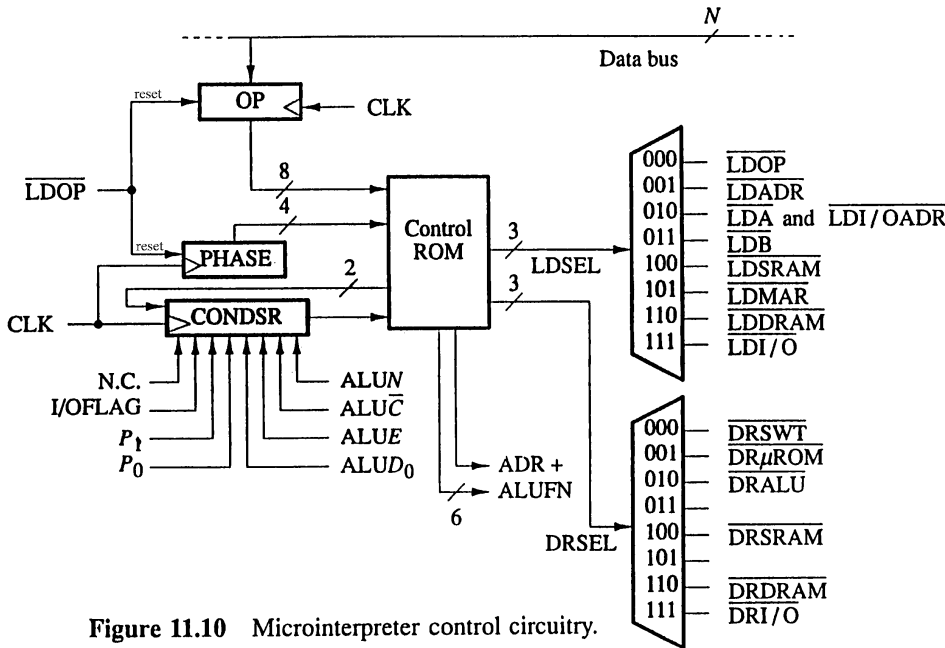


Figure 11.10 Microinterpreter control circuitry.

Table A2.4 Useful ALU functions.

Control inputs						Output
F ₃	F ₂	F ₁	F ₀	C̄	M	
0	0	1	1	1	1	00000000
1	1	0	0	1	1	11111111
1	1	1	1	1	1	A
1	0	1	0	1	1	B
1	1	1	1	1	0	A - 1
0	0	0	0	0	0	A + 1
1	0	0	1	1	0	A + B
0	1	1	0	0	0	A - B
1	0	1	1	1	1	A AND B
1	1	1	0	1	1	A OR B
0	1	1	0	1	1	A XOR B
0	0	0	0	1	1	Ā (1's complement)

Table A2.2 Condition shift register control inputs.

Inputs		Action
I	S	
0	0	Load condition register
0	1	Shift condition register right
1	0	No change
1	1	No change

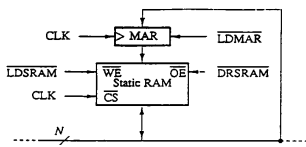


Figure 11.5 Static RAM subsystem.

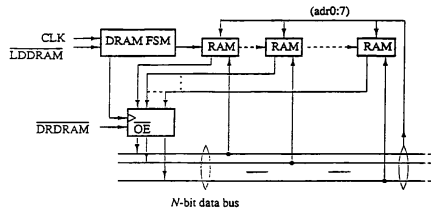


Figure 11.8 Main-memory (dynamic RAM) subsystem.

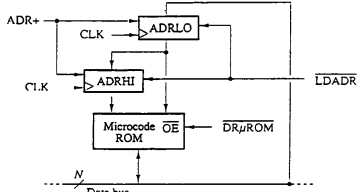


Figure 11.7 Microcode ROM with 16-bit address register.

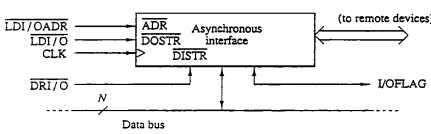


Figure 11.9 Communications interface.

Table A2.3 Function decoding: 74181 ALU inputs and functions.

Control inputs					Function performed if M = 0 (arithmetic)	Function performed if M = 1 (logical)
F ₃	F ₂	F ₁	F ₀			
0	0	0	0		A + 1 - C̄	Ā
0	0	0	1		(A OR B) + 1 - C̄	(A OR B)
0	0	1	0		(A OR B̄) + 1 - C̄	Ā AND B
0	0	1	1		-C̄	00000000
0	1	0	0		A + (A AND B̄) + 1 - C̄	(A AND B)
0	1	0	1		(A OR B) + (A AND B̄) + 1 - C̄	B̄
0	1	1	0		A - B - C̄	A XOR B
0	1	1	1		(A AND B̄) - C̄	A AND B̄
1	0	0	0		A + (A AND B) + 1 - C̄	Ā OR B
1	0	0	1		A + B + 1 - C̄	(A XOR B)
1	0	1	0		(A OR B) + (A AND B) + 1 - C̄	B
1	0	1	1		(A AND B) - C̄	A AND B
1	1	0	0		A + A + 1 - C̄	11111111
1	1	0	1		(A OR B) + A + 1 - C̄	A OR B̄
1	1	1	0		(A OR B̄) + A + 1 - C̄	A OR B
1	1	1	1		A - C̄	A